

General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

Features

- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

Application

- DC-DC
- Load Switch

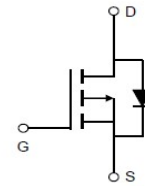
Ordering Information:

Part NO.	ZM900P10M
Marking	900P10
Packing Information	REEL TAPE
Basic ordering unit (pcs)	5000

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}	$25^\circ\text{C} \leq T_J \leq 175^\circ\text{C}$	-100	V
Gate-Source Voltage ^①	V_{GS}		± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	-10.6	A
	I_D	$T_C=75^\circ\text{C}$	-8.3	A
	I_D	$T_C=100^\circ\text{C}$	-6.8	A
Pulsed Drain Current	I_{DM}	Pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25^\circ\text{C}$;	-42.4	A
Total Power Dissipation	P_D	$T_C=25^\circ\text{C}$	35	W
Total Power Dissipation	P_D	$T_A=25^\circ\text{C}$	2.1	W
Operating Junction Temperature	T_J		-55 to +150	$^\circ\text{C}$
Storage Temperature	T_{STG}		-55 to +150	$^\circ\text{C}$
Single Pulse Avalanche Energy	E_{AS}	$L=0.1\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	50	mJ
		$L=0.5\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	105	mJ
ESD Level (HBM)	CLASS 2			

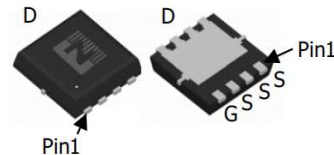
Product Summary



$$V_{DS} = -100\text{V}$$

$$R_{DS(ON)} = 110\text{m}\Omega$$

$$I_D = -10.6\text{A}$$



DFN3*3



•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	3.6	°C/W
Thermal resistance, junction-ambient ^②	R_{thJA}		-	60	°C/W
Soldering temperature (total time<10s)	Tsold		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	-100			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	-1.3	-1.8	-2.5	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS}=0V, V_{DS}=-100V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=-8A$		110	145	m Ω
		$V_{GS}=4.5V, I_D=-6A$		125	165	m Ω
Forward Transconductance	g_{FS}	$V_{GS}=5V, I_{SD}=-6A$		15		S
Diode Forward Voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=-8A$			1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1MHz, V_{DS}=-25V$	-	2330	-	pF
Output capacitance	C_{oss}		-	94	-	
Reverse transfer capacitance	C_{rss}		-	46	-	
Gate Resistance	R_g	$f=1MHz$	-	13		Ω
Total gate charge	Q_g	$V_{DD}=-15V, I_D=-8A, V_{GS}=-10V$	-	30	-	nC
	$Q_g(-4.5v)$		-	21	-	
Gate - Source charge	Q_{gs}		-	6.8	-	
Gate - Drain charge	Q_{gd}		-	3.3	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=-10V, V_{DS}=-15V, R_G=3.3\Omega, I_D=-10A$	-	8	-	ns
Turn-ON Rise time	t_r		-	16	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	55	-	ns
Turn-Off Fall time	t_f		-	30	-	ns

Fig.1 Gate-Charge Characteristics

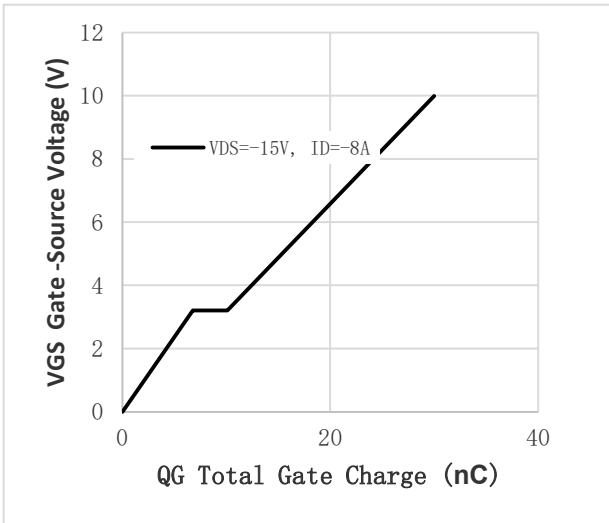


Fig.2 Capacitance Characteristics

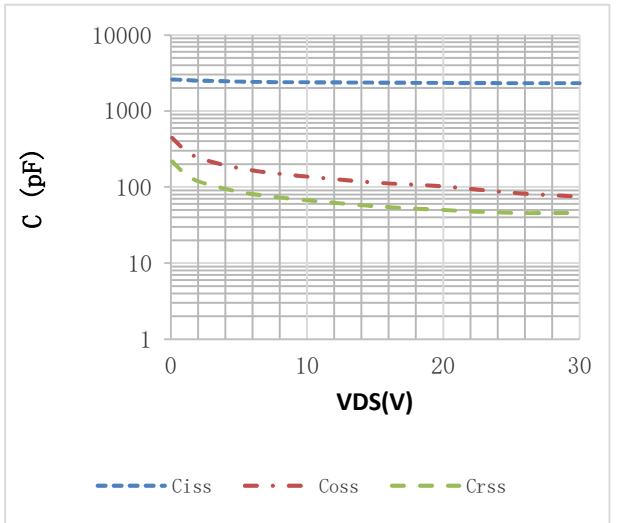


Fig.3 Power Dissipation

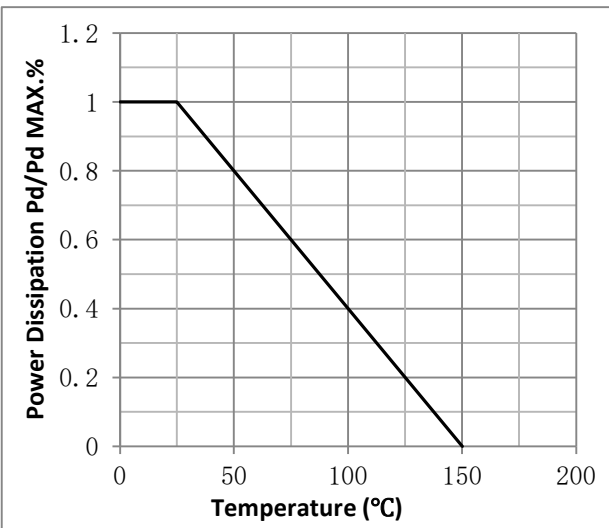


Fig.4 Typical output Characteristics

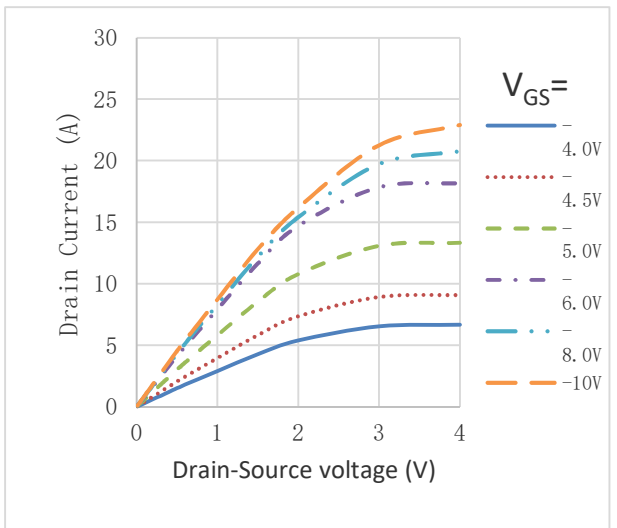


Fig.5 Threshold Voltage V.S Junction Temperature

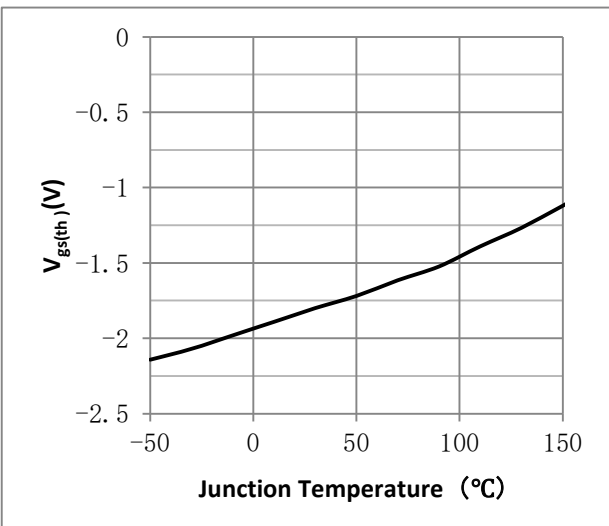


Fig.6 Resistance V.S Drain Current

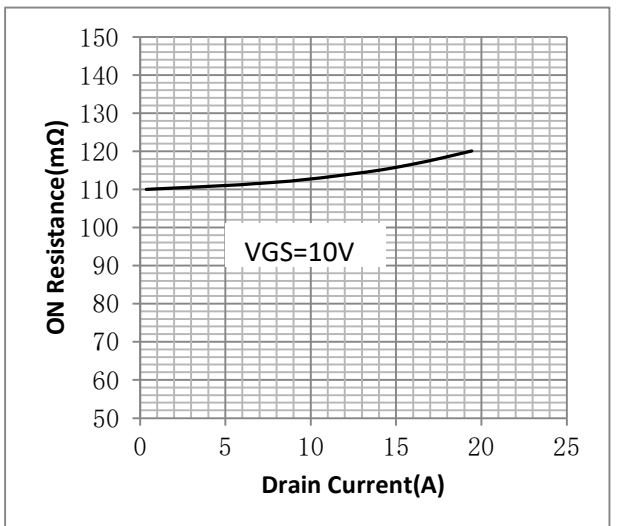


Fig.7 On-Resistance VS Gate Source Voltage

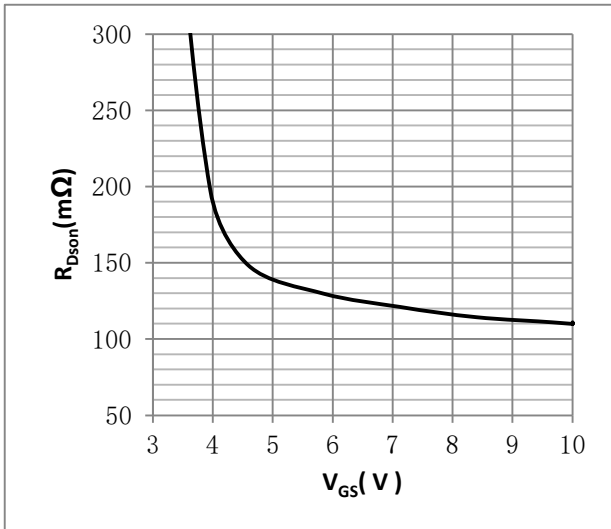


Fig.8 On-Resistance V.S Junction Temperature

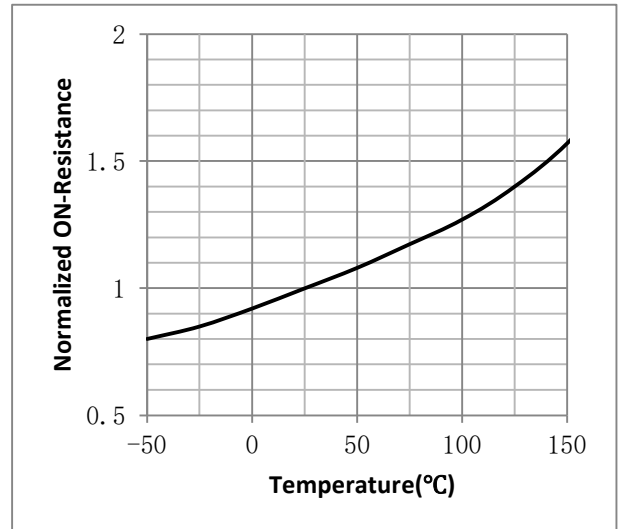


Figure 9. Diode Forward Voltage vs. Current

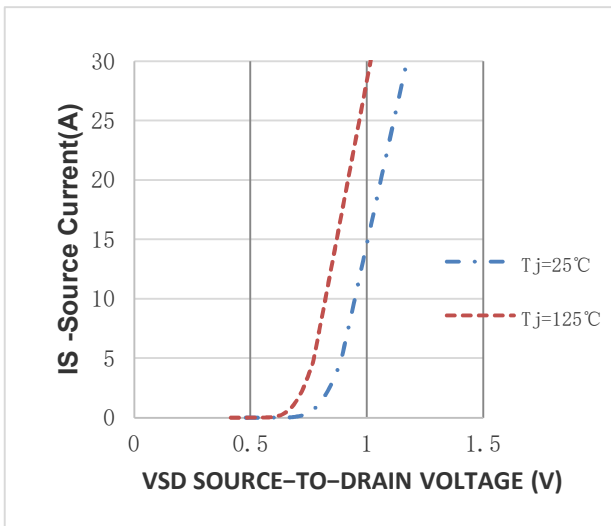


Figure 10. Transfer Characteristics

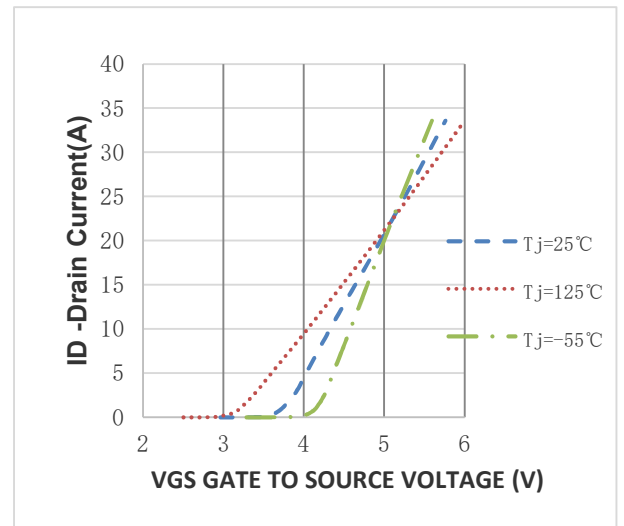


Fig.11 SOA Maximum Safe Operating Area

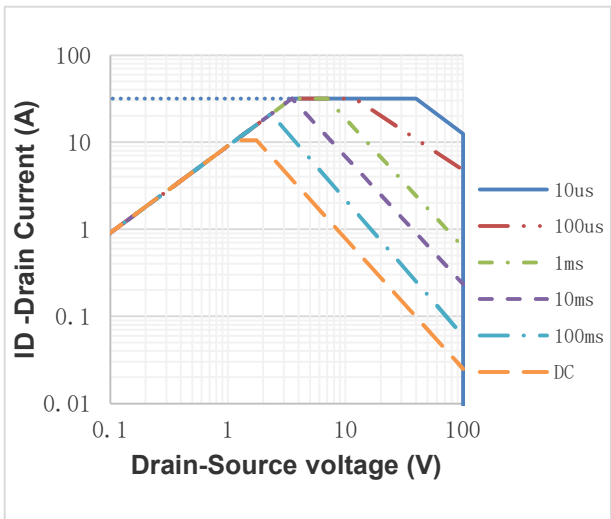
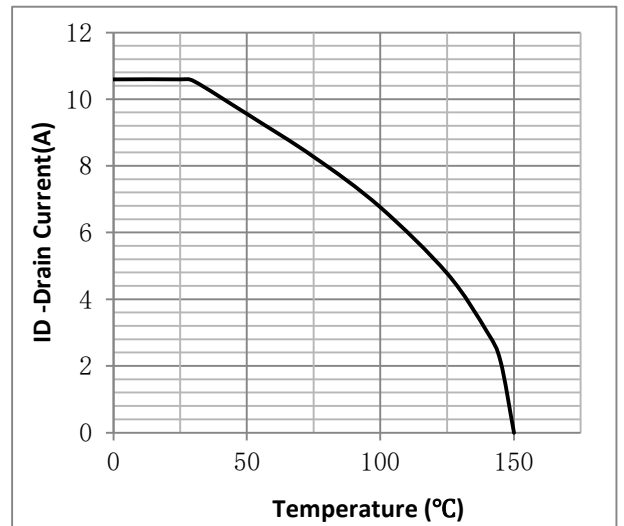
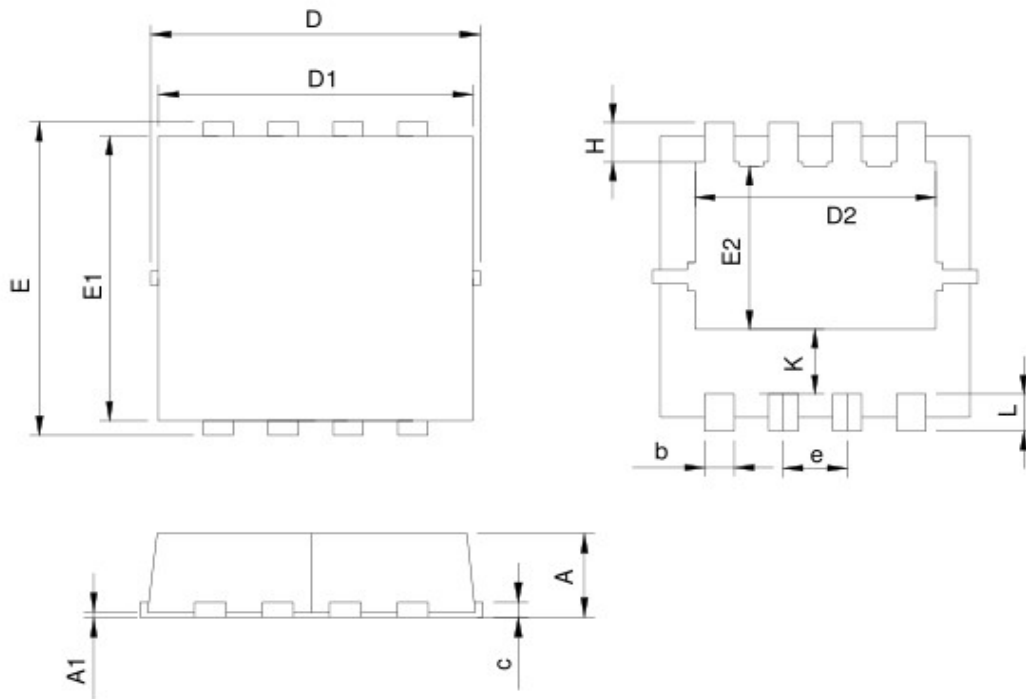


Fig.12 I_D vs. Case Temperature^③

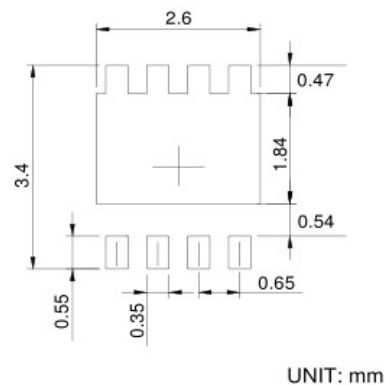


•DFN3*3 Package Outline



SYMBOL	DFN3.3x3.3-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.00	0.028	0.039
A1	0.00	0.05	0.000	0.002
b	0.25	0.35	0.010	0.014
c	0.14	0.20	0.006	0.008
D	3.10	3.50	0.122	0.138
D1	3.05	3.25	0.120	0.128
D2	2.35	2.55	0.093	0.100
E	3.10	3.50	0.122	0.138
E1	2.90	3.10	0.114	0.122
E2	1.64	1.84	0.065	0.072
e	0.65 BSC		0.026 BSC	
H	0.32	0.52	0.013	0.020
K	0.59	0.79	0.023	0.031
L	0.25	0.55	0.010	0.022

RECOMMENDED LAND PATTERN



Note:

- ① Pulse : $V_{GS}=+20V/-20V$, Duty cycle=50%, $T_j=175^{\circ}C$, $t=1000$ hours; For DC , the following test conditions can be passed: $V_{GS}=-20V/+10V$, $T_j=175^{\circ}C$, $t=1000$ hours ;
- ② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ③ Practically the current will be limited by PCB, thermal design and operating temperature. $V_{GS}=10V$.

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Revision History

Version	Date	Change
A	2021. 2. 3	
B	2022. 9. 7	1. Add Reach, HF figure, 2. ID modify
C	2024. 6. 20	Correct fig 3, 5, 8